CLAIMS

1. (Currently Amended) A method of etching an integrated circuit (IC) structure having an etched dielectric material with an exposed barrier layer, wherein said barrier layer is composed of a material ~~selected from a group consisting of~~ consisting essentially of silicon nitride ~~and silicon carbide~~, said method comprising:

   feeding a nitrous oxide (N_2O) gas and a fluoromethane (CH_3F) gas into a reactor;

   generating a plasma in said reactor;

   etching said barrier layer; and

   generating a high selectivity between said barrier layer to said dielectric material.

2. (Original) The method of claim 1 wherein said dielectric material is comprised of materials that include silicon and oxygen.

3. (Original) The method of claim 2 wherein said selectivity of said barrier layer to said dielectric is 1.7 or more.

4. (Original) The method of claim 1 wherein said etched dielectric material is composed of a material selected from the group consisting of silicon dioxide, silicon oxide, organosilicate glass, SiLK, and fluorinated silicate glass.

5. (Original) The method of claim 1 further comprising depositing a thin barrier layer over said IC structure.

6. (Currently Amended) A method of etching an integrated circuit (IC) structure having an etched first dielectric layer, a second barrier layer wherein said barrier layer is composed of a material ~~selected from a group consisting of~~ consisting essentially of silicon nitride ~~and silicon carbide~~, and a third layer having a copper interconnect, said barrier layer between said etched first dielectric layer and said third layer, comprising:

feeding a nitrous oxide (N_2O) gas and a fluoromethane (CH_3F) gas into a reactor;

generating a plasma in said reactor;

etching said barrier layer;

generating a high selectivity between said barrier layer to said dielectric material; and

limiting oxidation of said third copper interconnect.

7. (Original) The method of claim 6 wherein said selectivity of said silicon nitride barrier layer to said etched dielectric is 1.7 or more.

8. (Original) The method of claim 6 wherein said etched first dielectric material is composed of a material selected from the group consisting of silicon dioxide, silicon oxide, organosilicate glass, SiLK, and fluorinated silicate glass.

9. (Original) The method of claim 6 further comprising depositing a thin barrier layer over said IC structure.

10. (Currently Amended) A method of etching an integrated circuit (IC) structure having a via etched into a first dielectric layer composed of a first dielectric material, a second barrier layer wherein said barrier layer is composed of a material ~~selected from a group consisting of~~ consisting essentially of silicon nitride~~ and silicon carbide~~, and a third layer having a conductive interconnect surrounded by a second dielectric material that comprises silicon and oxygen, said barrier layer between said etched first dielectric layer and said third layer, comprising:

feeding a nitrous oxide (N_2O) gas and a fluoromethane (CH_3F) gas into a reactor;

generating a plasma in said reactor;

etching said barrier layer;

generating a high selectivity between said barrier layer to said first dielectric material and said second dielectric material; and

limiting oxidation of said third copper interconnect.

11. (Original) The method of claim 10 wherein said selectivity of said silicon nitride barrier layer to said etched dielectric is 1.7 or more.

12. (Original) The method of claim 11 wherein said first dielectric material is composed of a material selected from the group consisting of silicon dioxide, silicon oxide, organosilicate glass, SiLK, and fluorinated silicate glass.

13. (Original) The method of claim 12 further comprising depositing a thin barrier layer over said IC structure.

14. (Original) The method of claim 10 wherein via and said conductive interconnect are misaligned, and during said etching of said silicon nitride barrier layer, said second dielectric material is partially etched and a cavity is formed in said second dielectric material.

15. (Original) The method of claim 14 further comprising depositing a thin barrier layer over said IC structure that covers said cavity, said via and said trench.